LATENCY CONTROL CIRCUIT AND METHOD OF LATENCY CONTROL

RELATED APPLICATION DATA

This is a continuation-in-part of Application No. 10/283,124 filed October 30, 2002 (now U.S. Patent No. 6,707,759); the contents of which is hereby incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

[0001] Fig. 1 illustrates a block diagram of a prior art memory device. The memory device 100 includes a memory cell array 110, a clock synchronizing circuit block 120, a read command path block 130, a data output buffer 140, a mode register 150 and a latency circuit 160. In operation, data is written into the memory cell array 110 and read out from the memory cell array 110. If a read command is asserted to the memory device 100, data is read out from the memory cell array 110 according to an externally received address. A buffer 116 receives and temporarily stores the address. A row decoder 112 receives the stored address and decodes a row address of the memory cell array 110 from the address. A column decoder 114 receives the stored address and decodes a column address of the memory cell array 110 from the address. The memory cell array 110 outputs the data addressed by the row and column addresses. The data output buffer 140 receives the data output from the memory cell array 110, and outputs the data based on a latency signal from the latency circuit 160 and an internal data output clock signal CLKDQ.

[0002] The clock synchronizing circuit block 120 generates the data output clock signal CLKDQ based on an external clock signal ECLK. The external clock signal ECLK serves as a reference clock signal for